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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,610	03/17/2004	Hisakatsu Yamaguchi	108390-00061	1910

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EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
05/14/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

DCIPDocket@arentfox.com
IPMatters@arentfox.com
Patent_Mail@arentfox.com

Office Action Summary	Application No.	Applicant(s)	
	10/801,610	YAMAGUCHI, HISAKATSU	
	Examiner	Art Unit	
	YOUNG T. TSE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,17,19 and 21* is/are rejected.

7)☒ Claim(s) *11-16,18 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 31, 2008 has been entered.

Drawings

2. The drawings were received on March 31, 2008. These drawings are acceptable.

Claim Objections

3. Claim 21 is objected to because of the following informalities: in claim 21, line 2, the term “with sync a clock signal” should be “with a clock signal”. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-10 and 21 are rejected under 35 U.S.C. 102(a) as being anticipated by Hasako et al., U. S. Publication No. 2003/0093715 A1, hereinafter "Hasako".

Hasako discloses a block diagram illustrating an exemplary test apparatus 1 and an exemplary display device 3 in Figure 1. The test apparatus 1 comprises a test signal generation circuit 10 including a test pattern generation circuit 15, a clock generation circuit 16 and a jitter generation circuit 17; a test signal transmission circuit 11 including a data transmission circuit 18 and a phase modulation circuit 19; a control circuit 12; a control signal transmission circuit 13; and a control signal reception circuit 14. The display device 3 comprises a reception circuit 30 including a data reception related circuit 34 having a data reception circuit 38 and a PLL circuit 39; an inspection circuit 35 having an error information generation circuit 40 and a malfunction information generation circuit 41; an inspection result image generation circuit 37; and a display switching circuit 36; a display unit 31; a control signal transmission circuit 33; and a control signal reception circuit 32.

Figure 3 shows the detailed embodiment of the test pattern generation circuit 15 of Figure 1.

Figures 4 and 5 show two different embodiments of the data transmission circuit 18 of Figure 1.

Figure 6 shows the detailed embodiment of the phase modulation circuit 19 of Figure 1.

Figures 7 and 8 show two different embodiments of the data reception circuit 38 of Figure 1, wherein each of the data reception circuit 38 comprises at least a reception amplifier 380, a data comparator circuit 401 and a counter 402.

Regarding claims 1, 5 and 21, the test apparatus 1 comprises a clock generation circuit which may include the test pattern generation circuit 15, the clock generation circuit 16, the jitter generation circuit 17, and the phase modulation circuit 19 to generate a clock signal (clk3) generated from the phase modulation circuit 19 derived from clock clk1 and clk2 generated from the clock signal generation circuit 16 and the jitter generation circuit 17; a jitter generator which may include the jitter generation circuit 17 and the test pattern generation circuit 15 to generate jitter (clk2) in the clock signal based on a setting signal, which is a control signal controlled by the control circuit 12 to initialize the jitter signal generation circuit 17 to set a present condition of the jitter (paragraph [0331]); and the data transmission circuit 18 to transmit data (test signal) in sync with the clock signal including the jitter. Also see paragraphs [0222] to [0224].

In addition to claim 21, the data reception circuit 38 to receive the test signal and the clock signal including jitter, and measures a transfer condition of the test signal.

Regarding claims 2 and 6, the jitter generation circuit 17 and the test pattern generation circuit 15 adjust the amount of the frequency of the jitter included in the clock signal to reduce the frequency of the jitter.

Regarding claims 3-4 and 7-8, the test pattern generation circuit 15 generates a random PN pattern jitter in the clock signal during a test mode as shown in Figure 3.

Regarding claim 9, the data reception circuit 30 receives the transmitted test signal, the phase modulation circuit 19 also supplies a receive clock signal to the PLL circuit 39 of the data reception circuit 30; wherein the test apparatus 1 comprises the test pattern generation circuit 15 to generate a data pattern for a jitter resistance test and the data transmission circuit 18 allows the data pattern to be transmitted in sync with the clock signal (clk3); and the data reception circuit 30 comprise the data reception circuit 38 and the PLL circuit 39 to allow the data pattern transmitted by the data transmission circuit 18 to be received in sync with the received clock signal and the data comparator circuit 401 (see Figure 7 or Figure 8) to compare the data pattern received by the reception circuit 38 with an expectation value to output a comparison result.

Regarding claim 10, the comparison result from the data comparator circuit 401 is being stored in a counter 402 on an amount of the frequency of the jitter.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasako in view of Masuda et al., U.S. Patent No. 6,791,623, hereinafter "Masuda".

Regarding claims 17 and 19 as applied to claims 1 and 5 respectively, although Kasako does not explicitly show, teach or suggest that the test apparatus 1 further comprises a selector to select the clock signal clk3 or the received clock signal including the jitter based on a control signal, for example, by the control circuit 12.

Masuda discloses a selection circuit (733) in Figure 66 and teaches that the selection circuit (733) selects either a clock signal generated from the clock generator circuit (732) including jitter or a clock signal generated from the PLL circuit (731) including no jitter based on a control signal generated from the fitter detector (772) and the switch controller (771). See col. 47, lines 16-38.

Therefore it would have been obvious to one of ordinary skill in the art to comprise a selector or switch circuit in Hasako's test apparatus to select the clock signal, for example, the transmitted clock signal provided to the data transmission circuit of the test apparatus 1 or the received clock signal provided to the data reception circuit of the display device 3 as taught by Masuda in order to synchronize the test signal of the test apparatus 1 and the received test signal of the display device 3.

Allowable Subject Matter

8. Claims 11-16, 18 and 20 would be allowable if rewritten to overcome the objections set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is 571- 272-3051. The examiner can normally be reached on Monday-Friday 10:00-6:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on 571- 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/YOUNG T. TSE/
Primary Examiner, Art Unit 2611